REMARKS

Claims 1-12 were examined and reported in the Office Action. Claims 1-5 are rejected. Claim 1 is amended. Claims 6-12 are withdrawn.

Applicant requests reconsideration of the application in view of the following remarks.

I. 35 U.S.C. § 103(a)

It is asserted in the Office Action that claims 1-5 are rejected in the Office Action under 35 U.S.C. § 103(a), as being unpatentable over U. S. Patent No. 6,780,756 issued to Farber et al ("Farber"), in view of U. S. Patent No. 6,329,230 issued to Matsuda ("Matsuda"). Applicant respectfully traverses the aforementioned rejection for the following reasons.

According to MPEP §2142 "[t]o establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." (In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)). Further, according to MPEP §2143.03, "[t]o establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)." *"All words in a claim must be considered* in judging the patentability of that claim against the prior art." (In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970), emphasis added.)

Applicant's amended claim 1 contains the limitations of "[a] semiconductor device comprising: a semiconductor substrate; source and drain electrodes, which are

formed on the semiconductor substrate to make ohmic contact with the semiconductor substrate; a T-shaped gate electrode, which is formed between the source and drain electrodes on the semiconductor substrate; a first insulating layer formed on the semiconductor substrate and is in direct contact with the source electrode, the drain electrode and the T-shaped gate electrode; a silica aerogel layer formed on the first insulating layer; and a second insulating layer formed on the silica aerogel layer, the source electrode and the drain electrode, the second insulating layer including silica aerogel, the second insulating layer is directly in contact with the T-shaped gate electrode."

Applicant notes that in the Office Action mailed on October 6, 2004 acknowledgement of Applicant's claim for foreign priority was made and that all certified copies of the priority documents have been received. Applicant's foreign priority date is November 26, 2002, which invalidates Farber as being prior art.

Even though Applicant asserts that Farber is improper prior art, Applicant submits the following. Farber discloses a metal layer of a back-end module where the height of the interconnects is greater than the height of the dielectric regions. It is asserted in the Office Action that Farber discloses "a first insulating layer (21) formed on the semiconductor substrate." (Office Action, page 2, section 1). Thin dielectric layer 21, however, is formed between the dielectric regions 20, which are not formed on substrate 7. Therefore, Farber does not teach, disclose or suggest a first insulating layer formed on the semiconductor substrate. Applicant, however, has amended claim 1 for clarification by adding the limitation "a first insulating layer formed on the semiconductor substrate and is in direct contact with the source electrode, the drain electrode and the T-shaped gate electrode," which is clearly not taught, disclosed or suggested by Farber.

Further, it is asserted Farber discloses that the second insulating layer is coupled to the T-shaped gate electrode." Therefore, Applicant has amended claim 1 for clarification by adding the limitation of "the second insulating layer including silica

aerogel, the second insulating layer is directly in contact with the T-shaped gate electrode," which is not taught, disclosed or suggested by Farber.

Matsuda discloses a semiconductor device including a gate structure formed on a substrate where a lightly doped drain (LDD) structure is formed. Matsuda is relied on in the Office Action for disclosing a T-shaped gate electrode. Matsuda, hover, does not teach, disclose or suggest "a first insulating layer formed on the semiconductor substrate and is in direct contact with the source electrode, the drain electrode and the T-shaped gate electrode," or "the second insulating layer including silica aerogel, the second insulating layer is directly in contact with the T-shaped gate electrode."

Even if Farber is combined with Matsuda, the resulting invention would still not teach, disclose or suggest "a first insulating layer formed on the semiconductor substrate and is in direct contact with the source electrode, the drain electrode and the T-shaped gate electrode," or "the second insulating layer including silica aerogel, the second insulating layer is directly in contact with the T-shaped gate electrode." Therefore, there would not be any motivation to combine the two.

Further, Applicant submits that by viewing the disclosure of Farber combined with Matsuda, one can not jump to the conclusion of obviousness without impermissible hindsight. According to MPEP 2142, [t]o reach a proper determination under 35 U.S.C. 103, the examiner must step backward in time and into the shoes worn by the hypothetical 'person of ordinary skill in the art' when the invention was unknown and just before it was made. In view of all factual information, the examiner must then make a determination whether the claimed invention 'as a whole' would have been obvious at that time to that person. Knowledge of applicant's disclosure must be put aside in reaching this determination, yet kept in mind in order to determine the 'differences,' conduct the search and evaluate the 'subject matter as a whole' of the invention. The tendency to resort to 'hindsight' based upon applicant's disclosure is often difficult to avoid due to the very nature of the examination process. However, impermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art." Applicant submits that

without first reviewing Applicant's disclosure, no thought, whatsoever, would have been made to have "a first insulating layer formed on the semiconductor substrate and is in direct contact with the source electrode, the drain electrode and the T-shaped gate electrode," or "the second insulating layer including silica aerogel, the second insulating layer is directly in contact with the T-shaped gate electrode."

Neither Farber, Matsuda, nor the combination of the two teach, disclose or suggest the limitations contained in Applicant's amended claim 1, as listed above. Since neither Farber, Matsuda, nor the combination of the two teach, disclose or suggest all the limitations of Applicant's claim 1, there would not be any motivation to arrive at Applicant's claimed invention. Thus, Applicant's claim 1 is not obvious over Farber in view of Matsuda since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claims that directly or indirectly depend from claim 1, namely claims 2-5, would also not be obvious over Farber in view of Matsuda for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for claims 1-5 are respectfully requested.

CONCLUSION

In view of the foregoing, it is submitted that claims 1-5 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: June 7, 2005

By: _____
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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail with sufficient postage in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P. O. Box 1450, Alexandria, Virginia 22313-1450 on June 7, 2005

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Jean Svoboda